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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 09/921,561 | 08/06/2001 | Kazufumi Komura | 024016-00012 | 7046 |

7590 03/11/2004

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| EXAMINER | |
|---|---|
| NGUYEN, MINH T | |
| ART UNIT | PAPER NUMBER |
| 2816 | |

DATE MAILED: 03/11/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/921,561 | KOMURA ET AL. | |
| | Examiner | Art Unit | |
| | Minh Nguyen | 2816 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *13 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1,10,11,18,21-23,26,32 and 35-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1,10,11,18,26,35 and 36* is/are allowed.

6)☒ Claim(s) *32 and 37* is/are rejected.

7)☒ Claim(s) *21-23* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 August 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Continued Examination Under 37 CFR 1.114*

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 12/29/03 has been entered.

### *Claim Rejections - 35 USC § 103*

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 32 and 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 5,778,214, issued to Taya et al.

As per claim 32, Taya discloses a delay circuit (Fig. 12) comprising:

a delay section having two or more delay stages (11a, 11b, ...) connected in series (as shown), each has an input (for receiving the signal) and an output (for outputting the delayed signal), each stage adds a predetermined delay time (this is the delay time of the corresponding delay stage); and

selecting switch means (12a, 12b, ...) connected as recited (each input of the switch 12(i) receives the signal output from each of the corresponding delay stage 11(i)) for establishing a delay path from the input signal so that the output signal has a desired delay time (by selecting the switch 12(i), the signal from the SIGNAL INPUT TERMINAL is delayed a desired delay time at the SIGNAL OUTPUT TERMINAL).

Taya does not explicitly disclose the delay signal coming from each of the delay stage 11(i) has substantial uniform rise delay time and fall delay time as called for in the claim.

However, Taya explicitly teaches the delay element 12(i) is implemented using CMOS inverters (column 9, lines 41-42) and he further teaches a difference between rise time and fall time of the signal outputted from a CMOS gate can be achieved by changing the driving capabilities of the CMOS transistors (column 9, lines 66-67 and column 10, lines 1-2).

As understood by a person skilled in the art, mass production of transistors having the same driving capabilities has the most cost advantage since these transistors have the same size.

The examiner takes Official Notice the fact that using the same size transistors for implementing CMOS inverters, the rise time and fall time of the output signal from that inverter would be substantially uniform.

It would have been obvious to one skilled in the art at the time of the invention was made to implement the Taya delay stages using the same sizes transistors for the advantage of minimizing the cost.

As per claim 37, this claim is rejected for the same reason and motivation noted in claim 32.

***Response to Arguments***

3. Applicant's arguments with respect to the claims have been considered but are moot in view of the new ground(s) of rejection and/or the amended claims are allowed.

***Allowable Subject Matter***

4. Claims 1, 10-11, 18, 26 and 35-36 are allowed.

Claims 1, 10-11, 18 and 35-36 are allowed because the prior art of record fails to disclose or suggest the inclusion of the limitation "the delayed input signal is propagated to each gate of the first and second transistors via the selecting section means" as recited in claim 1. The recited limitation clearly requires the selecting switch section having the structure shown in Fig. 6 of the present invention, i.e., the delayed input signal (N10) is propagated to the gates of T11 and T12 via NAND gate 12 and NOR gate 11.

Claim 26 is allowed for the reason noted in claim 1.

5. Claims 21-23 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 21-23 are allowable because the prior art of record fails to disclose or suggest the inclusion of an even number of logic inversion sections wherein each logic inversion section having different propagation delay time between the rise and fall transition in each of the delay stages as recited in claim 21.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Minh Nguyen whose telephone number is 571-272-1748. The examiner can normally be reached on Monday, Tuesday, Thursday, Friday 7:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

3/4/04

Minh Nguyen
Primary Examiner
Art Unit 2816